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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
LINDSAY JR, WALTER LEE	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,122	KU ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6,19,20 and 23-25 is/are rejected.

7)☒ Claim(s) 7-18 and 22 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/28/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Election filed on 10/06/2004.

Currently, claims 1-25 are pending.

Election/Restrictions

Restriction has been withdrawn.

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

2. Claims 7-19 and 23-25 are objected to because of the following informalities: in claim 7, line 3 a colon should appear after "includes"; in claim 14, line 4 a colon should appear after "of"; in claim 19, line 3 a colon should appear after "includes"; and in claim 23, line 3 "and" should be removed, in line 4 a semicolon should appear after "insulator", in line 6 a colon should appear after "including", and in line 8 a semicolon should appear after "silicon". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 23-24 rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (U.S. Patent No. 6,277,722 dated 8/21/2001).

Lee shows the structure as claimed, in Figs. 1-4 and corresponding text as: a semiconductor substrate (10)(col. 2, lines 50-61); a gate insulator (11) formed on the semiconductor substrate(col. 2, lines 50-61); and a metal gate pattern (20) formed on the gate insulator(col. 2, lines 50-61); the metal gate pattern having a top surface and substantially vertical sidewalls and including: a first conductor pattern (12) formed on the gate insulator, the first conductor pattern including silicon (col. 2, lines 50-61); a second conductor (14) pattern formed on the first conductor pattern, the second conductor pattern including a metal (col. 2, lines 50-61); and a capping layer (30)(nitride film) configured and arranged on the sidewalls of the metal gate pattern (col. 3, lines 1-5), whereby a first oxidation rate of the first conductor pattern is enhanced relative to a second oxidation rate of the second conductor pattern (col. 3 lines 34-37)(claim 23) Lee teaches that the first conductor pattern includes polysilicon (col. 2, lines 50-61); and the second conductor pattern includes tungsten (col. 2, lines 50-61)(claim 24).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims1-6, 19-20 and 25 are rejected under 35 U.S.C. 103(a) as being obvious over Lee et al. (U.S. Patent No. 6,277,722 dated 8/21/2001) in view of Kobayashi et al. (U. S. Patent No. 4,505,028 dated 3/19/1985).

Lee shows the method and structure substantially as claimed, in Figs. 1-4 and corresponding text and as previously described including: forming a gate insulating layer (11) having an initial thickness on a silicon substrate (10) (col. 2, lines 50-61) ; depositing a metal gate material on the gate insulating layer, the metal gate material (12, 13, 14) including at least one metal layer; etching the metal gate (13, 14) (col. 2, lines 50-61); etching the metal gate material to form a metal gate pattern (20) (col. 2, lines 62-67); forming a capping layer (30) (nitride film, oxidation prevention layer) on the

metal gate pattern (col. 3, lines 1-5); oxidizing at least a portion of the silicon substrate without substantially oxidizing the at least one metal layer and without substantially increasing the initial thickness of the gate insulating layer (reoxidation)(col. 3, lines 24-37) (claims 1 and 25). Lee teaches that the metal gate material includes a polysilicon layer (col. 2, lines 50-61); oxidizing at least a portion of the silicon substrate also oxides a portion of the polysilicon layer (reoxidation)(col. 3, lines 24-37) (claim 2). Lee teaches that the gate insulating layer includes at least one insulating material layer selected from the group consisting of silicon oxide, silicon oxynitride, silicon nitride, metal oxides and metal silicates (col. 2, lines 50-61) (claim 3). Lee teaches that the metal layer is selected from the group consisting of W, Ni, Co, TaN, Ru-Ta, TiN, Ni-Ti, Ti-Al-N, Zr, Hf, Ti, Ta, Mo, MoN, WN, Ta-Pt and Ta-Ti (col. 2, lines 50-61) (claim 4). Lee teaches that the metal gate pattern has a stacked structure selected from the group consisting of metal/barrier metal/polysilicon/gate insulator stack, a metal/polysilicon/ gate insulator stack, a metal barrier metal/ gate insulator stack and a metal/gate insulator stack, (col. 2, lines 50-61) (claim 5). Lee teaches that the metal gate pattern is formed of a gate mask (15)/tungsten/tungsten nitride/polysilicon/ gate insulator stack, (col. 2, lines 50-61) (claim 6). Lee teaches that forming the capping layer includes: forming a silicon nitride layer on a portion of the surface of the semiconductor substrate and the top surface and sidewall of the metal gate pattern (Fig. 2), the silicon nitride layer being formed under conditions such that the at least one metal layer remains substantially unoxidized (col. 3, lines 1-5) (claim 19).

Lee lacks anticipation only in not explicitly teaching that: 1) at least a portion of the silicon substrate is selectively oxidized without substantially increasing the initial thickness of the gate insulating layer (claims 1 and 25); 2) selectively oxidizing at least a portion of the silicon substrate also oxides a portion of the polysilicon layer (claim 2); and 3) selectively oxidizing the at least one metal uses a wet oxidation process utilizing partial pressures of H_2O and H_2 (claim 20).

Kobayashi teaches a method for producing a semiconductor device with a metal gate structure. Kobayshi utilizes partial pressures of H_2O/H_2 that selectively oxidizes Si without substantially oxidizing W or Mo (col. 3, lines 7-39). Kobayashi teaches that the mechanism at work in the partial pressure H_2O/H_2 atmosphere will reduce W to its metallic state without reducing the Si (col. 3, lines 1-6). This characteristic is advantageous for fabrication of MOS transistors having high integration density (col. 3, lines 56-62).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify the method and structure shown in Lee selectively oxidizing at least a portion of the silicon substrate without substantially increasing the initial thickness of the gate insulating layer and oxides a portion of the polysilicon layer, by using a wet oxidation process utilizing partial pressures of H_2O and H_2, as taught by Kobayashi with the motivation that Kobayashi teaches that mechanisms at work in the partial pressure H_2O/H_2 atmosphere reduce W to its metallic state without reducing the Si. Additionally, this mechanism aids in the fabrication of MOS transistors having high integration density.

8. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (U.S. Patent No. 6,277,722 dated 8/21/2001) in view of Kobayashi et al. (U. S. Patent No. 4,505,028 dated 3/19/1985) as applied to claim 1 above, and further in view of Hwang et al. (U.S. Patent No. 6,245,605 dated 6/12/2001).

Lee as modified by Kobayashi shows the method substantially as claimed and as described in the preceding paragraphs.

Lee as modified by Kobayashi lack anticipation only in not explicitly teaching that: 1) implanting impurity ions into the portion of the silicon substrate using the metal gate pattern as an ion implantation mask after the portion of the silicon substrate has been selectively oxidized (claim 21).

Hwang teaches a method for producing a semiconductor device with a metal gate structure. Hwang shows a light selective thermal oxidation that forms a poly-smile oxidation (118) (col. 4, lines 17-32). Then drain extension (119) implants are implanted into the substrate (col. 4, lines 33-45). This is done in order to selectively form an oxide in the presence of a metal without significantly oxidizing the metal (col. 2, lines 20-22).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify the method shown in Lee as modified by Kobayashi, by implanting impurity ions into the portion of the silicon substrate has been selectively oxidized, with the motivation that Hwang teaches that an oxide is formed selectively in the presence of a metal, without significantly oxidizing the metal.

Allowable Subject Matter

9. Claims 7-18 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...forming the capping layer includes:

forming a silicon oxide layer on a surface of the semiconductor substrate and a top surface and sidewalls of the metal gate pattern, the silicon oxide layer being formed under conditions such that the at least one metal layer remains substantially unoxidized, as required by claim 7, as it depends on claim 1;

...the silicon oxide layer included in the capping layer has a thickness of not more than about 500 Å, as required by claim 8, as it depends on claim 7;

...injecting a nitrogen source gas into the reaction chamber, the conditions in the reaction chamber being sufficient to cause the nitrogen source gas to form a nitrogen atmosphere within the reaction chamber; and

injecting a silicon source gas and an oxygen source gas into the reaction chamber under conditions sufficient to cause the silicon oxide layer to form on the metal gate pattern, as required by claim 9, as it depends on claim 7;

...the nitrogen atmosphere is substantially free of oxygen, as required by claim 10, as it depends on claim 9;

...the nitrogen source gas includes ammonia, as required by claim 11, as it depends on claim 10;

...the silicon source gas includes at least one source gas selected from a group consisting of SiH_4, Si_2H_6, DCS, TCS and HCD; and

the oxygen source gas includes at least one source gas selected from a group consisting of N_2O, NO and O_2, as required by claim 12, as it depends on claim 9;

...the injection of the silicon source gas is initiated at a time no later than the injection of the oxygen source gas is initiated, as required by claim 13, as it depends on claim 9;

...the injection of the nitrogen source gas into the reaction chamber is terminated under a condition selected from a group consisting of: after the injection of the oxygen source gas has been initiated, substantially simultaneously with the initiation of the oxygen source gas, and before injection of the oxygen source gas or injection of the silicon source gas has been initiated, as required by claim 14, as it depends on claim 9;

...forming the silicon oxide layer includes a chemical vapor deposition process selected from a group consisting of plasma enhanced CVD, remote plasma enhanced CVD, high density plasma CVD, thermal CVD, laser CVD and hot filament CVD, as required by claim 15, as it depends on claim 9;

...etching the silicon oxide layer to form silicon oxide spacers on the sidewalls of the metal gate pattern, as required by claim 16, as it depends on claim 7;

...depositing a silicon nitride layer on the silicon oxide layer, as required by claim 17, as it depends on claim 7;

...etching the silicon nitride layer to form silicon nitride spacers on the silicon oxide layer formed on the sidewalls of the metal gate pattern, as required by claim 18, as it depends on claim 17; and

...the metal gate pattern has a width of not more than about 100 nm;

the capping layer has a thickness of not more than 150 Å; and

the initial thickness of the gate insulating layer is increased by less than 10Å, as required by claim 22, as it depends from claim 2.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL

November 15, 2004